42,44 (i.e., of a conductivity which is the opposite of the source and drain). CMOS devices may have both n-channel and p-channel in adjacent regions of a substrate.

(2) Please amend the paragraphs at page 7, lines 1-31 as follows:

A voltage adjust implant is performed while the n-well tub is defined. Dopant atoms, such as boron, are implanted into an upper region of the n-well 14 in the region at which the gate is to be formed to define a p-channel implant as shown in FIGURE 2. This implant is referred to as the threshold adjust implant and is used to set the threshold voltage at the gate. Preferably, the boron threshold adjust implant provides a nominal turn on (about 0.4 volts for 0.16 μm technology) for to-be-defined channel 30 in both PMOS and NMOS devices.

The gate 22 layers are then deposited. Specifically, an oxide for the gate oxide layer 28 is grown over the substrate surface, for example, by thermal oxidation. Polysilicon for the gate 22 is then deposited over the gate oxide. Various techniques, such as physical deposition, chemical vapor deposition, or epitaxial growth, may be used to perform this step. Preferably, an upper layer 33 of tungsten silicide, is then deposited over the polysilicon, by, for example, sputtering.

A layer 60 of a hard mask material is then deposited on an upper surface of the gate -i.e., on an upper surface 62 of the tungsten silicide layer 33. The mask material is one which is etched selectively over polysilicon or silicon. The hard mask material is preferably an oxide, such as silicon oxide, or silicon nitride. However, other oxides which are deposited by chemical vapor deposition (CVD) may also be used. The silicon oxide may be formed, for example, by LPCVD or PECVD using a plasma comprising tetraethylorthosilicate (TEOS), and optionally hydrogen, to a thickness of between about 500 and 2000Å, preferably, about 1000-1500Å.